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DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE – RAIGAD -402 103

Winter Semester Examination – December - 2019

Branch: B. Tech. (E & TC Engineering/Electronics Engineering) **Sem.:- III**

Subject with Subject Code:- Digital Logic Design (BTEXC305) **Marks: 60**

Date:- 19/12/2019 **Time:- 3 Hr.**

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Instructions to the Students

1. Each question carries 12 marks.
2. Attempt **any five** questions of the following.
3. Illustrate your answers with neat sketches, diagram etc., wherever necessary.
4. If some part or parameter is noticed to be missing, you may appropriately assume it and should mention it clearly

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Q. No. 1a) Design Four bit Binary to Gray Code Converter. **(06)**

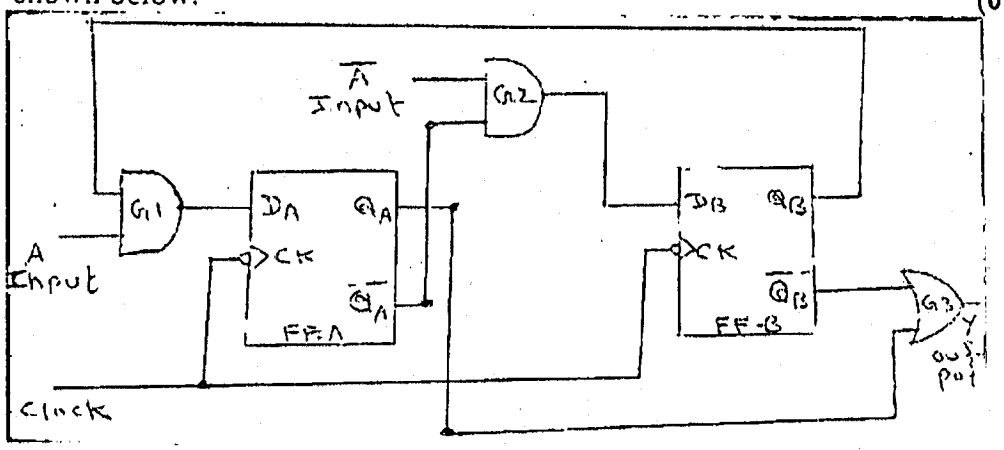
b) Implement the three-variable Boolean function:
$F(A, B, C) = \dot{A}.C+A.\dot{B}.C+A.B.\dot{C}$ using 8-to-1 multiplexer. **(06)**

Q. No. 2a) Convert T Flip-Flop to D Flip-Flop. **(06)**

b) Design a three bit synchronous Up/Down counter using JK Flip-Flop. **(06)**

Q. No. 3a) Design a sequence detector to detect the sequence .....110.....(Use Mealy Machine with JK FF). **(06)**

b) Derive the state table & state diagram for the sequential Moore circuit shown below. **(06)**



Q. No. 4a) Explain the various characteristics of Digital IC's. **(06)**

b) Draw the circuit diagram of two input TTL NAND gate with Totem pole output and explain its working. **(06)**

Q. No. 5a) Implement the following Boolean function using suitable PLA.
$F(A,B,C.D) = \sum m(3, 4, 5, 7, 10, 14, 15)$ **(06)**

b) Draw the interfacing diagram showing the interface of four memory

integrated circuits each of size 2K x 4 bits to get the desired memory size of 4K x 8 bits. **(06)**

Q. No. 6a) Write down VHDL code for full adder using Data flow model with necessary diagram. **(06)**

b) List the various advantages and features of VHDL. **(06)**

Paper End